REMARKS

The Applicant has filed the present Response in reply to the outstanding Official Action of October 20, 2004, and the Applicant believes the Response to be fully responsive to the Official Action for reasons set forth below in greater detail.

At the onset the Applicant would like to note that Claims 1-4, and 21-23 have been amended. Specifically, the claims have been amended to recite a test circuit for a semiconductor integrated circuit device. Additionally, Claim 1 has been amended to include limitations regarding the structure of the two-pulse generator. Claim 2 has been amended to recite that the test circuit is fabricated in the semiconductor integrated circuit device. Claim 3 has been amended to recite that the test circuit is mounted on a test board, and the semiconductor integrated circuit device is removably mounted on the test board. Claim 4 has been amended to further describe structural features of the test circuit, namely, that the circuit further comprises a PLL circuit for multiplying the frequency of the test clock and supplying a signal having the multiplied-frequency to the two-pulse generator. Amended Claims 21 and 23 contain similar subject matter, in that both further limit the structure of the test circuit; however, Claim 21 depends from Claim 3, whereas Claim 23 depends from Claim 1. No new matter has been added by the aforementioned amendments. Support for such amendments can be found on pages 4-6, and 8 as well as Figure 7.

Additionally, these amendments do not require any new search by the Examiner. For example, the amendment to the body of Claim 1 incorporates subject matter that was in original dependent Claim 3; the amendment to Claim 3 incorporates subject matter that was in original Claim 21. Further, amended Claim 4 has similar subject matter as original Claim 2.

The claims of the instant application are patentably distinct from Jaber et. al. (hereinafter "Jaber"). Jaber discloses a test circuit (LSSD) which reduces power dissipation by stopping a test clock during scan operation. LSSDCLK 403 which is asynchronous to

COP_CLKG211 controls whether to output or to stop outputted from CLKG205. This in turn causes a change in the number of clocks output from CLKG205. This structure does not allow for two clock pulses to be outputted precisely.

In stark contrast, the present invention is designed to provide exactly two clock pulses which have the same interval as the test clock for enabling path delay testing between scan flip-flops. The two clock pulses are generated by a two-pulse generator which is controlled by a gate signal generator. The claimed invention is directed to a test circuit which precisely controls the number of clock pulses by stopping the output of the clock after the two-pulse generator generates two clock pulses, effectively extracting only two-clock pulses having the same interval as the test clock from the test clock. The test circuit is fabricated in the semiconductor-integrated circuit device. The prior art reference does not teach these features.

Additionally, since the purpose of the prior art is solely to reduce power dissipation by completely stopping the clock when it is not needed, it is neither necessary nor suggested to control the number of clock pulses precisely.

Therefore, the configuration of the present invention is not identical with the configuration of the prior art. Additionally, the invention is not obvious in view thereof because of the problems solved by the prior art and the present invention are completely different. There would be no motivation or suggestion to modify the prior art reference to arrive at the claimed invention.

In conclusion, the Applicant believes that the above-identified application is in condition for allowance and henceforth respectfully solicits the Examiner to allow the application. If the Examiner believes a telephone conference might expedite the allowance of this application, the Applicant respectfully requests that the Examiner call the undersigned, Applicant's attorney, at the following telephone number: (516) 742-4343.

Respectfully submitted,

Seth Weinfeld
Registration No: 50,929

SMW:al